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EXAMINER	
TIMORY, KABIR A	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/779,845	FUJII, NORIO	
	Examiner	Art Unit	
	Kabir A. Timory	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. This office action is in response to the amendment filed on July 18, 2007. Claims 5-7 are added. Claims 1-7 are pending in this application and have been considered below.

Response to Arguments

2. Applicant arguments regarding the rejection under 35 USC 102(b) as being anticipated by Ohzeki et al. (US Patent Number 4,625,241) have been fully considered but they are not persuasive. The examiner thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meets the claimed limitation as rejected.

(1) Applicant's arguments: "Ohzeki *et al.* fails to disclose a counter circuit to which the digitized input signal, a counter clock signal and a trigger signal are provided so as to set a count number based on the digitized input signal and start counting the counter clock signal in response to the trigger signal, as required by independent claim 1".

The examiner's response: The cited reference "Ohzeki et al." as a whole discloses all the limitation of independent claim1. In figure 5, Ohzeki et al. discloses a

first start signal (FSTRT) signal, which reads on a trigger signal, a sampled clock signal (CK), which are generated by the SYNC CKT (block 41 in figure 5), and a digital signal is output from ROM 43. FSTRT is input in the CLEAR input of counter 48, the digital input signal is input to the D input of flip-flop 44, and CK is input in CK input of flip-flop 44. The flip-flop 44 and clock counter 48 together constitute the counter circuit as recited in claim1. Therefore, according to figure 5, it is clear that the reference discloses a counter circuit (44 and 48 in figure 5) to which the digitized input signal, a counter clock signal and a trigger signal are provided so as to set a count number based on the digitized input signal and start counting the counter clock signal in response to the trigger signal, as required by independent claim 1. Furthermore, in column 5,lines 20-68, Ohzeki et al. describes the entire operation of figure 5, which contains the all of the limitation of claim 1.

Applicants are reminded that the rejection is made based on the entire content of the cited prior art.

3. Applicant's arguments with respect to claims 5-7 have been considered but are moot in view of new ground(s) of rejection because of the amendment.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 5, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohzeki et al. (US Patent Number 4,625,241).

Regarding claim1:

Ohzeki et al. discloses a timing adjusting apparatus comprising:

- an AD converter (A/D converter in figure 5) for receiving an input signal of which input signal level is converted into a digital signal to generate a digitized input signal (input waveform is interpreted to be input signal) (column 2, lines 59-65); and
- a counter circuit (figure 6, 57) to which the digitized input signal, a counter clock signal (44 and 48 in figure 5) and a trigger signal (FSTRT is interpreted to be the trigger signal) (FSTRT in figure 5, column 5,lines 20-68) are provided so as to set a count number based on the digitized input signal and start counting the counter clock signal in response to the trigger signal (column 5,lines 20-68), wherein an output signal is generated from the counter circuit at the timing of the counter clock signal reaching the count number (44 and 48 in figure 5, column 5,lines 20-68).

Regarding claim 2:

Ohzeki et al. further discloses the digitized input signal is set as the count number when the trigger signal is input (column 4, lines 37-41).

Regarding claim 5:

Ohzeki et al. further discloses wherein said input signal is determined by an adjusting time which delays an output timing of the output signal with regard to the trigger signal (FSTRT, CK1 and CK2 in figure 4).

Regarding claim 6:

Ohzeki et al. further discloses wherein said counter clock signal is supplied to the counter circuit continuously irrespective of timings of the digitized input signal or the trigger signal being supplied thereto (the CK signal in figure is supplied to the system which is interpreted to be in continuous manor) (CK in figure 5).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohzeki et al. (US Patent Number 4,625,241) in view of Sakuragi et al. (US Pub Number 2002/0109620).

Regarding claim 3:

Ohzeki et al. discloses said AD converter is further comprising:

a binary-coded N-bit output counter for counting an input clock signal and carrying out a

count operation repeatedly (figure 6, 57);

a latch circuit for inputting the N-bit output signal as data, latching the N-bit output signal, and outputting the latched N-bit output signal as the digitized input signal in accordance with a change of the comparison output signal (figure 6, 55).

Ohzeki et al. discloses all of the subject matter as described above except for specifically teaching a DA converter for converting an N-bit output signal of the binary-coded N-bit output counter into a counter analog signal, and outputting the counter analog signal; a comparator for comparing the input signal with the counter analog signal to output a comparison output signal.

However, Sakuragi et al., in the same field of endeavor, teaches a DA converter for converting an N-bit output signal of the binary-coded N-bit output counter into a counter analog signal (figure 1, 2), and outputting the counter analog signal; a comparator for comparing the input signal with the counter analog signal to output a comparison output signal (figure 1, 3).

One of ordinary skill in the art would have clearly recognized that in order to convert the output of the counter to a digital signal a D/A "digital to analog" converter is required. Furthermore, to compare the analog input signal with the output signal of the D/A converter to control the counter in accordance with the comparison result a comparator is added to the system. In order to convert the analog output of a counter and to compare the analog output with digital output, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a D/A converter

along with a comparator as taught by Sakuragi et al. in doing so we can attain accuracy in the system.

Regarding claim 4:

Ohzeki et al. further discloses, the counter clock signal is selected from one of the N-bit output signals (figure 6, 56, column 6, lines 45-49).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohzeki et al. and Sakuragi et al. as applied to claim 4 above, and further in view of Yoshikawa et al. (US Patent Number 4,745,588)

Regarding claim 7:

Ohzeki et al. and Sakuragi et al., discloses all of the subject matter as described above except for specifically teaching wherein said counter clock signal is selected from one of N-bit output signals in accordance with a rotation of a disk.

However, Yoshikawa et al., in the same field of endeavor, teaches wherein said counter clock signal is selected from one of N-bit output signals in accordance with a rotation of a disk (column 6, lines 54-64, and column 7, lines 47-50).

One of ordinary skill in the art would have clearly recognized that in optical disk circuits, counters are used adjust the timing index signal of a optical disk.

In order to adjust the timing of an optical disk, it would have been obvious to one

ordinary skill in the art at the time the invention was made to include a counter to counts the clock pulses in accordance with the optical disk rotation as taught by Yoshikawa et al. in controlling the tracking of an optical disk by moving an objective lens and a carriage supporting the objective lens.

Including a counter that counts the number pluses in accordance with optical disk rotation is advantageous because it provides a timing adjustment for the system.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kabir A. Timory whose telephone number is 571-270-1674. The examiner can normally be reached on 6:30 AM - 3:00 PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kabir A. Timory
September 20, 2007

Shuwang Liu

SHUWANG LIU
SUPERVISORY PATENT EXAMINER